176_23_CS_Z_R0-4-RE1-4

Recruitment App Link

https://webapps.bsc.es/recruitment/job/2528

Website Node ID

60774

Job Reference

176_23_CS_Z_R0-4-RE1-4

Position

Research Engineer/Researcher - Software/hardware engineers for emerging technologies (RE1-4/R1-4/R0)

Closing Date

Sunday, 30 June, 2024
Reference: 176_23_CS_Z_R0-4-RE1-4
Job title: Research Engineer/Researcher - Software/hardware engineers for emerging technologies (RE1-4/R1-4/R0)

About BSC

The Barcelona Supercomputing Center - Centro Nacional de Supercomputación (BSC-CNS) is the leading supercomputing center in Spain. It houses MareNostrum, one of the most powerful supercomputers in Europe, was a founding and hosting member of the former European HPC infrastructure PRACE (Partnership for Advanced Computing in Europe), and is now hosting entity for EuroHPC JU, the Joint Undertaking that leads large-scale investments and HPC provision in Europe. The mission of BSC is to research, develop and manage information technologies in order to facilitate scientific progress. BSC combines HPC service provision and R&D into both computer and computational science (life, earth and engineering sciences) under one roof, and currently has over 900 staff from 55 countries.

Look at the BSC experience:
BSC-CNS YouTube Channel
Let's stay connected with BSC Folks!

We are particularly interested for this role in the strengths and lived experiences of women and underrepresented groups to help us avoid perpetuating biases and oversights in science and IT research. In instances of equal merit, the incorporation of the under-represented sex will be favoured.

Context And Mission

The Barcelona Supercomputing Center (BSC) www.bsc.es is embarking on an umbrella of large-scale projects to contribute in the BSCs next generation supercomputer, the Marenostrum 6 (MN6), which will be operational in 2028/2029. In this ambitious and potentially rewarding endeavor, we need engineers and computer scientists at all levels of expertise (from 0 to 20+ years) and in both software and hardware fields. The final team will be around 100 engineers and scientists. The applicants would ideally have experience/ambition in at least one or more of the following fields:

· System software (operating system), including the development of new Linux services, tools, and drivers. Service visualization and containerization. Good understanding of the Linux kernel.
· Compilers, including the development of the LLVM compiler to target new features and/or optimizations (aimed at improving the performance of applications that are currently exploiting the RISC-V ISA).
· Parallel libraries and runtimes, including the development of new features and extensions in parallel library/runtime's systems for HPC programming models (e.g., MPI, OpenMP, SyCL), and workflow executions (e.g., COMPSs).
· Parallel numerical frameworks, including the use and development of numerical libraries (e.g., BLIS, OpenBLAS), and data analytic frameworks (e.g., Pythorch, Tensor Flow).
· HPC analysis, including the performance analysis of HPC applications, as well as the development of new tools (e.g., Extrae/Paraver) and benchmarks that may help to characterize the system behavior.
· HPC application engineering, including the understanding of actual scientific HPC applications (usually written in C/C++ and Fortran), and the development of modifications/extensions that may improve their performance.
· HPC resource awareness, including a good understanding of the underlying resource utilization and management in terms of nodes, processors, and memory (e.g., Slurm, DLB, Elasticity, DMRLib,...).
· Hardware engineering, including processor architecture and micro-architecture, accelerators, memory hierarchy, memory controllers, HBM, FPGA's, RTL design, VHDL, verilog, System C, System Verilog, place and route, timing closure, verification, validation, CI, post-silicon debug, DFT, and gate-level simulation

Key Duties

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Requirements

- Education
  - Junior profiles: BS or MS in Computer Science, Computer Engineering or Electrical Engineering. Previous industrial experience is a big plus.
  - Mid-level profiles: PhD in Computer Sciences, Computer Engineering or Electrical Engineering.
  - Senior profiles: PhD in Computer Sciences, Computer Engineering or Electrical Engineering.

- Essential Knowledge and Professional Experience

    - Junior profiles: Experience in industry is a big plus.
    - Mid-level profiles: 5+ year experience in industry in a leading role.
    - Senior profiles: 10-20+ years in industry in a leading role.

- Additional Knowledge and Professional Experience
    - Fluency in English is essential, Spanish is optional (free lessons available after joining)
    - Opportunity to enroll in Master or PhD program of UPC Computer Architecture Department.

- Competences
    - Planification and Organization
    - Ability to work individually and in a team
    - Innovation

Conditions

- The position will be located at BSC within the Computer Sciences Department
- We offer a full-time contract (37.5h/week), a good working environment, a highly stimulating environment with state-of-the-art infrastructure, flexible working hours, extensive training plan, restaurant tickets, private health insurance, support to the relocation procedures
- Duration: Open-ended contract due to technical and scientific activities linked to the project and budget duration
- Holidays: 23 paid vacation days plus 24th and 31st of December per our collective agreement
- Salary: we offer a competitive salary commensurate with the qualifications and experience of the candidate and according to the cost of living in Barcelona
- Starting date: asap

Applications procedure and process

All applications must be made through BSC website and contain:

- A full CV in English including contact details
- A Cover Letter with a statement of interest in English, including two contacts for further references - Applications without this document will not be consideredIn accordance with the OTM-R principles, a gender-balanced recruitment panel is formed for every vacancy at the beginning of the process. After reviewing the content of the applications, the panel will start the interviews, with at least one technical and one administrative interview. A profile questionnaire as well as a technical exercise may be required during the process.The panel will make a final decision and all candidates who had contacts with them will receive a feedback with details on the acceptance or rejection of their profile.At BSC we are seeking continuous improvement in our recruitment processes, for any suggestions or feedback/complaints about our Recruitment Processes, please contact recruitment [at] bsc [dot] es [dot] For more information follow this link

Deadline

The vacancy will remain open until a suitable candidate has been hired. Applications will be regularly reviewed and potential candidates will be contacted.

OTM-R principles for selection processes

BSC-CNS is committed to the principles of the Code of Conduct for the Recruitment of Researchers of the European Commission and the Open, Transparent and Merit-based Recruitment principles (OTM-R). This is applied for any potential candidate in all our processes, for example by creating gender-balanced recruitment panels and recognizing career breaks etc.
BSC-CNS is an equal opportunity employer committed to diversity and inclusion. We are pleased to consider all qualified applicants for employment without regard to race, color, religion, sex, sexual orientation, gender identity, national origin, age, disability or any other basis protected by applicable state or local law.
For more information follow this link
Barcelona Supercomputing Center - Centro Nacional de Supercomputación

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